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A FAST TURN AROUND FACILITY FOR VERY LARGE SCALE INTEGRATION (VLSI)

A SEMI-ANNUAL TECHNICAL STATUS REPORT

July 1, 1981 to December 31, 1981

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In order to appreciate the critical hardware and software problems associated with the definition and design of very large scale integrated circuits or integrated systems including 10^4 - 10^6 transistors in a single silicon chip, incisive experiments conducted with actual operating chips are indispensible. The objective of this project is to establish, within a university research environment, a facility for the rapid execution of mask generation, wafer fabrication, and functional testing of user-generated custom I.C. designs.

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Research Project

A FAST TURN-AROUND FACILITY

FOR VERY LARGE SCALE INTEGRATION (VLSI)

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The Stanford Fast Turn-Around Laboratory wafer fabrication activity is back in operation after a lengthy shut-down due to the re-construction of the building air handling system. Virtually all wafer fabrication equipment is once again functional and we have completed three NMOS "tune-up" runs to re-establish our process capability. During the shut down, many significant improvements were made which are aimed specifically at increasing the process integrity and decreasing the defect density of the fabricated NMOS wafers. Details of these improvements are included at the end of this report. Key pieces of new equipment which are now functional and are presently being incorporated into the standard process secquence are a cassette-load photoresist coat/bake/develop system, a plasma etch system for anisotropically etching polycrystalline silicon, and low pressure chemical vapor deposition of silicon nitride (with polycrystalline silicon and phosphorus glass in the check-out phase).

Activity in the area of process development has focussed on a 2 micron CMOS technology. Features of this technology are a 400 Å gate oxide a 4 micron deep n-well, a p^+ junction depth of 0.6 micron, and an n^+ junction depth of 0.35 micron. A detailed electrical performance evaluation chip has been designed and masks are currently being fabricated. Important test structures on this design include detailed transistor characterization structures with gate lengths as small as 1 micron, both NMOS and CMOS ring oscillators for direct speed comparisons, and a wide variety of latch-up structures. Because our current in-house emulsion mask making facility cannot provide the required resolution for these structures, masks are being E-Beam written at Perkin-Elmer ETEC. While awaiting these masks, we have begun a run which will allow us to characterize in detail the performacne of the p-channel transistors fabricated in wafers which have a "blanket" n-well.

The ETEC MEBES machine has arrived at Stanford and is currently undergoing initial checkout of the facility particle and temperature control. Initial checkout of the patterning capability should begin shortly. In joint activities with Perkin-Elmer ETEC, work is underway on a lanthanum hexaboride electron source which will provide improved brightness for a 1/8 micron writing capability, and on a planarizing tri-level resist technology which will be required for direct-write lithography capability.

Much of the recent testing ativity has focussed on incorporating the Tektronix S3260 functional test system into the family of testers (i.e. the minimal and the medium testers) which are driven by the ICTEST language. Recent accomplishments include the augmentation of the ICTEST language to provide the timing information required by the S3260 test system and establishment of a communications link between the S3260 and the Tektronix test system. Several designs have been tested at speed using the ICTEST/S3260 system. Additional details of the testing ativity are included at the end of this report.

FTAF WAFER FABRICATION

This was a period of significant enhancement to the processing facility at the expense of a shut down of actual processing activity. This shut down was dictated by the need to totally renovate the exhaust system in the McCullough Building to handle present and future processing activities. The McCullough bulding was not originally designed to handle the large amount of exhaust required by IC processing equipment, and it had gotten to the point where no additional equipment could be installed in the IC Lab located in the basement. With this renovation, the total exhaust for the IC Lab was increased from 3600 to 36,000 CFM. In addition to the exhaust system, this shut down offered the opportunity to renovate the whole IC Lab to better meet the FTAF program goals over the next two years until the new CIS building is ready. The upgrades accomplished during this period included improved process utilities, better particle control, and a conversion to a 3" wafer capability.

Process Utilities - A new service pad was installed outside. This allowed the remote installation of a new DI water system with three times the flow, a bulk nitrogen tank, and miscellaneous other support equipment. Previously all these functions had been located within the basement of the McCullough building. This addition was important since it made room for the installation of the new MEBES system in the IC Lab, and it provided the DI water and N_2 required to upgrade the lab from 2" to 3" wafer capability.

Particle control - A number of steps were taken to reduce the airborne particle count in the lab , which reduces defects on fabricated chips. An incoming air system with high efficacy particle (HEPA) filters was installed for the IC Lab making the whole area class 10,000 worst case. Offices were removed form the processing area so that limited control access could be initiated, thus reducing the people flow and associated particle generation.

New diffusion, lithography and etching areas were installed so that the FTAF effort could have separate restricted processing areas with tighter particle control than required by other less critical activities in the lab. These new areas are in addition to the space allocated for the installation of the new MEBES system. However, the new lithography area will include the processing activities associated with MEBES and will use the *** MEBES slowing room for entry. In these new FTAF areas, 19 laminar flow stations with HEPA filters were installed to bring the room particle counts in these areas below 1,000 and the bench counts below 10.

3" Wafers Capability - Until this shut down the lab could only process 2" wafers. This was a severe problem because it is difficult to get high quality 2" wafers, and most of the newer equipment needed to fabricate VLSI chips will not handle 2" wafers. In addition, larger wafers offer a better yield and more chances of producing defect-free chips. A 3" conversion was chosen over going to 4" since a number of existing pieces of equipment could be modified to take 3" wafers, but not 4". All new equipment being purchased is being specified to be easily convertibale up to 5" for future flexibility. The conversion from 2" to 3" wafer processing capability was accomplished by modifying the existing ion implanter and E-beam metal systems, by installing 3" furnace tubes and wet stations and by modification of miscellaneous other items in the lab.

The modification to the ion implanter consisted of designing, fabricating and installing a eight position 3" wafer carousel end station which bolted onto the existing 2" research end station. This station features manual load and auto advance. The main drawback with this station and the present implanter is that a source/drain implant can take up to 1 hour per wafer. While this time is not desirable, it is a livable situation until we have enough time and manpower to install a new implanter with a greater current.

The modification to the E-beam metal deposition system consisted of adding a 3" wafer planet to hold 3" wafers and adding a scanner circuit to the power supply to make the E-beam scan across the source. This latter modification will improve metal step coverage.

The new 3" furnaces which were installed and characterized consist of two 3-stack furnace banks (6 tubes total) with manual load. New features incorporated are automatic mass flow control for all gases, in-situ process thermocouples for monitoring wafer temperature, H_2/O_2 steam generation, TCA bubblers for in-situ HCl tube cleaning, a $POCl_3$ bubbler temperature controller for precise phosphorus diffusions, programmable dual temperature set point for temperature ramping, programmable sequencer control and "White Elephant" boat loading capability for particle control. These features are a significant enhancement over our previous furnace capability and will be critical to our fabrication of small geometry large area chips. Initial results are showing 1% uniformity in oxide thicknesses, and 2% uniformity in doping and improved breakdown characteristics. The tube arrangement for these furnaces consists of a phosphorus tube, a boron tube, 3 oxidation tubes, and a forming gas anneal tube.

Three new wet stations for cleaning and wet etching of 3" wafers were designed for industrial type processing with teflon cassettes, hot pots, dump rinsers and spin dryers. In the past the IC Lab has used quartz wafer holders, hot plates, beakers, and N_2 blow dry. This change over was dictated by the awkwardness of the old method for larger wafers, improved particle control and the need to reduce operator dependence of wafer cleaning. The arrangement of these stations consists of one bench in the diffusion area set up for wafer cleaning with a dedicated spin dryer and two wet stations next to each other in the new etching room with dedicated positions for nitride, oxide, aluminum

etching and positions for resist stripping of metallized and non-metallized wafers. These last two stations share a spin dryer. The justification for improving the wet etching capability when the dry etching needs are so strong is that wet etching is needed as a base line and backup as dry etching processes are brought under control.

Two additional wet stations were installed in the new lithography area. One of these is set up for MEBES plate processing and the other is set up for experimental resist processes.

New equipment - The following new processing equipment arrived: A nitride low pressure chemical vapor deposition (LPCVD) system, a low temperature doped oxide LPCVD system, a furnace for poly LPCVD, a tungsten LPCVD system, and a Nanospec thin film measurement system. In addition, orders were placed for an auto resist processing system and a poly plasma etching system.

The poly, nitride and oxide LPCVD systems will be significant enhancements to our processing capability. The presently used atmospheric pressure processes have uniformity, particle and cross-contamination problems. By going to the proven technology of dedicated low pressure systems these problems should be overcome. The tungsten system is a research activity of looking at tungsten as replacement for, or an addition to the presently used aluminum layer.

The auto resist system is part of our upgrade to 3" wafer capability. It will offer wafer resist coating, baking, and positive resist development. The poly plasma etcher is an automated etcher dedicated to poly and nitride etching. It is specified to have both anisotropic and isotropic etching capabilities. Both the resist system and the etcher are microprocessor controlled and have wafer cassette load. We are looking for these features in all new equipment in order to gain better process and particle control.

Facility

During this period we continued to plan the facility for MEBES. We decided to use a vertical laminar flow enclosure around the work table for optimum temperature control and particle cleanliness. The alternative would have been an environmental chamber with horizontal laminar flow, although this approach may be less expensive, we felt that it would have jeopardized system performance. However, ????????????? with Perkin-Elmer Etec (Now Perkin-Elmer E.B.T.) and Fairchild, Amdahl, and IBM.

On September 1, a letter was sent out from Stanford's facilities design and engineering group with invitations to bid on the construction of this facility. However, we continued to have trouble with the contractor doing the design package on which the project would be bid. Because of incomplete details in these plans, the facilities office decided in mid-November to go another route, using these existing plans as a starting point. This new route would have an architect redesign the facility and a construction manager supervise the actual work in McCullough. We felt that this route will save both construction time and money over the original plan with its needed change orders. Ehrlich-Rominger was selected as the architect and Howard J. White was selected as the construction manager. We met with these firms on severaloccasions and had a design review submittal meeting on December 21; the design looked good. White's cost estimate for the construction at that point was $411 K.

Substantial completion of this project is scheduled for 26 April, 1982, with MEBES delivered from P.E. on March 15. A conservative estimate for the

MEBES to pass the site acceptance tests identical to the factory acceptance tests passed in February '81, is about three months from installation. Following that, we are scheduled to have the LaB_6 gun installed. This will take approximately one month, during which we will have partial use of the machine.

Contracts with P.E. for Further Machine Development

a) LaB_6

During this period we negotiated the costs and performance for the development contract for the LaB_6 gun with Perkin Elmer E.B.T. This is a cost sharing, cost-plus-fixed-fee contract with an estimated cost to Stanford of $62,142. The acceptance tests for the LaB_6 gun follow. The details of the contract for the 1/8 micron capability are still under discussion. The present projected costs billed to Stanford are less tha #117,000.

Processing Area

Equipment such as the Solitec spray developer and bake ovens has started to arrive for the processing of E-Beam plates. The room adjacent to the MEBES room has been set aside for this purpose. The final equipment layout has not been specified since the space will be shared with VLSI photolithography and projection alignment equipment. We plan to get PBS resist (positive) processing on line as soon as possible so that its characterization will not be in a critical time path.

Multi-Level Resists

Ongoing work with P.E. is to develop a tri-level resist process for direct write with a thin sensitive E-Beam resist as the top layer. The bottom layer will form a planarizing layer so that the top layer can be thin for high resolution. The major problem is the reactive ion etch equipment needed to transfer the lithographic patterns into the thick bottom layer. We are awaiting the outcome of this equipment selection to purchase our own RIE plasma gear. $50 K has been set aside for this.

ACCEPTANCE TESTS FOR LaB_6 GUN

Performance and acceptance tests will be performed at Stanford's site after successful development and installation of LaB_6 source capability onto Stanford's MEBES (29). The designed performance objectives will be measured using the following methods:

The 0.125 μm spot size (12-88%) at 5 nA will be measured using the procedures in paragraph 3.38 of the MEBES operations manual (A910-3200C).

Spot current will be measured by scanning over an edge and measuring the transmitted current--AESOP.

Spot Current	Voltage	Diameter (12-88%)
5 nA	20 kV	0.125 μm
20 nA	10 kV	0.25 μm
40 nA	20 kV	0.25 μm
80 nA	10 kV	0.5 μm
160 nA	20 kV	0.5 μm
320 nA	10 kV	1.0 μm
600 nA	20 kV	1.0 μm

Spot drift will be measured after 4 hours of continuous operation of the column.

At no time during tests will the uncorrected beam current at the target drift by more than 1% over 1 hour.

The instrument shall perform the set of acceptance tests from the schedule for standard configuration with added tests for 0.125 μm as specified below.

	FAC 1	160 nA, 1.0 μm Market		
	FAC 2	40 nA, 0.5 μm Market		
	FAC 3	10 nA, 0.25 μm Market		
(new)	FAC 4	2.5 nA, 0.125 μm Market		
	FAC 5	PBS Test Plate	0.25 μ	
	SUDW 50	80 nA	75 mm diameter wafers written in	
	SUDW 25	20 nA	2 level with rotation between levels;	
(new)	SUDW 12	5 nA	10 wafers. SUDW 12 is SUDW 25 scaled by 0.5 for 0.125 μm spot size	

The LaB_6 gun will be installed immediately upon completion of the site acceptance tests of our standard MEBES.

FTAF TESTING

During the report period, meetings were held and test strip designs undertaken which culminated in the production of a new process verification test strip for use at Stanford. Coordinating meetings were held with participants from JPL, ISI, DARPA, Caltech, and Stanford. In these meetings, the currently used test structures were discussed and analyzed, with an eye towards designing an improved set for use at Stanford. The current process verification test strips got particular attention to find which structures gave the most useful data, and what desireable structures should be added. General information was collected on other dropin test chip designs, with anticipation of potential use in the detailed electrical test structures at Stanford. The decision was made to divide these test structures into several classifications, consisting of 1) Process test strip, 2) Detailed electrical test chip, 3) SPICE parameter extraction test chip, and 4) Yield test chips.

The process test strip is intended to have the minimum pad count and complexity necessary to allow verification of the successful completion of the process steps for fabrication of a custom design. This strip would be included in the die pattern for each group of a project group. The detailed electrical test chip provides those structures most useful for characterizing the secondary properties of interest in the NMOS process, such as polysilicon line propagation times, flip-flop operation speeds, and dynamic circuit node storage times. The SPICE parameter extraction chip incorporates those special structures of most value for computation of the many parameters needed for accurate SPICE model generation. The yield test chips would include large area structures with reduncance features that enable piecewise test of many types of dynamic and static structures optimized for particular defects.

These circuits contain features that permit isolation of measured defects to the areas of interest, and detect errors in the supporting structure.

A new process verification test strip has been designed as a result of the above studies, and is shown in Figure 1. This strip is based on the use of a probe card with two rows of ten probes, spaces 160 microns apart vertically and horizontally, making contact to metal pads that are 80 microns square. As the strip is configured, the probe card has to be moved several times to evaluate all of the test structures. Structure (1) contains a 20 micron square Van der Paw resistance test square, together with three resistors for measuring edge definition effects. These resistors are 4 terminal designs giving 10 squares of resistance, with horizontal units of width 20 and 5 microns, and a vertical unit of 5 micron width. Both orientations are provided to check for anisotropic etching effects. Structure (1) is for measuring the diffusion layer, while structures (4) and (5) measure the polysilicon and metal layers, respectively.

Structure (2) is a 19 stage ring oscillator for measuring the ultimate speed and power of the process. This circuit incorporates separate power connections to the oscillator and pad driver stages, with a high output current pad driver to enable easy measurement of the oscillation frequency in simple probing situations with heavy parasitic loading. Use of this oscillator gives a quick and easy measure of the relative dynamic performance to be expected from any given wafer run.

Structure (3) is a gate capacitor over a simulated enhancement transistor channel. There is a polysilicon gate region measuring 160 by 200 microns over a diffusion mask opening of 200 by 240 microns. Metal contacts are provided all around the periphery of the diffusion region so that high frequency capacitance measurements are more accurate due to lower series resistance.

Surrounding the entire structure is a polysilicon guard ring, which can be used to prevent surface inversion from affecting the measurement of the diffusion area capacitance to the substrate.

Structure (6) is a group of 14 transistors for obtaining basic electrical parameters of each type of transistor produced by the process. There are four groups of 3 transistors, each group containing W/L sizes of 10/5, 5/5, and 5/10 microns. These are for determination of the transistor true electrical sizes and conduction characteristics. Groups are provided for enhancement, native, depletion, and deep depletion transistors. In addition, there are two transistors measuring 50 microns square for quick determination of enhancement and depletion characteristics of a unit size device.

Structure (7) contains two groups of 3 field threshold transistors. One group has polysilicon gates, and the other uses metal gates. These transistors have W/L ratios in each group of 50/10, 50/5, and 50/2.5 microns. The objective here is to determine the maximum allowable overcrossing voltage for each case to check the effect of design rule changes, and to measure the variation of punchthrough voltage.

Structure (8) contains 3 four terminal contact resistance test structures. These test the contact resistance for metal to diffusion, metal to polysilicon, and polysilicon to diffusion. Some pads are shared to minimize the total pad count.

Structure (9) contains two inverters, one with a ratio of 4 and the other with a raio of 8. The ratio 8 inverter is provided with a pass transistor in series with its input so that this important test case can be checked. The inverters share input, ground, and power pads, with separate control of the pass gate and separate outputs.

After assembling this test strip, concern focusses on the amount of silicon real estate used for it, which would preclude use on every die of a

project set. It is a design goal that after the fabrication and use of this strip to bring the NMOS fabrication process back on line, the device structures and count will be examined closely. The objective will be to find those items which are most essential, and use them to form a new test strip of smaller size. Part of the present size came from use of subsections in a cellular manner, which although good for easy changing of the design, causes extra pads to be required. The optimized strip will use pad sharing as much as possible to minimize the total size, together with multipurpose structures where possible.

The question of which test structures to use for SPICE model parameter enhancement was studied, and a die location allocated in the new test mask for this purpose. After some thought, it was decided to give this chip design to Don Ward, who works in the transistor modeling group under Dr. Dutton, due to his familiarity with the needs of SPICE models. He will provide us with specifications for the structures he feels will give the most useful information.

Various possibilities for yield test structures were considered, taking the restrictions of the current techniques for test chip fabrication into account. Some of the possibilities include large ROM and RAM arrays, and specialized structures for checking specific types of defects. The use of standard structures was considred, but not felt to be the best way to go since fault isolation might be difficult. For the purpose of yield testing and defect statistics determination, the first test mask set will use the MATRIX chip design which was recently developed here at Stanford. This chip provides on a 3 mm square die an 8 by 8 matrix of test cell locations on 250 micron centers, together with the support logic necessary for addressing and reading out the cells. This logic is constructed so that it is possible to isolate

the occurrence of curcuit faults to either the support matrix or to the cell under test. Generally, this is accomplished with redundant readout circuits and voting logic, set up so that isolated faults in the circuits surrounding the cell of interest can be found and ignored. There is the additional capability of bypassing the active circuits in the cell of interest, to give additional verification of the proper cell accessing and readout. The cell structures presently available for MATRIX are a 29 stage ring oscillator and a two phase ratio type dynamic shift register. Additional cells will be designed in the future for selective testing of simpler structures.

During the present report period, the Tektronix S3260 test system was finally brought to a complete state of operation, with the requisite air conditioning installed to permit continuous operation without overheating its surrounding room. An experiment has been performed which verified the feasibility of converting the S3260 to run under the UNIX operating system. One of the Tektronix editor programs, originally run under the TEKTEST operating system, was successfully converted and run under UNIX on the VAX. As a result of this feasibility demonstration, the necessary hardware was ordered for augmenting the S3260 CPU capabilities to permit local use of UNIX. This includes 128K of memory, an RK07 disk interface, additional serial interfaces, and a GPIB controller for use with the X-Y prober. These are scheduled to be installed in the Spring when all items are on hand. Additionally, the required modifications for the ICTEST language to efficiently support the TEK-VAX interface and give two phase operation of the S3260 were defined. The ICTEST program has been modified in accordance with the requirements of the new timing discipline notation. Finally, an RS232 communication link, incorporating new hardware, has been developed to support preliminary operation of ICTEST on the S3260. Debugging of the link software and machine interfaces is

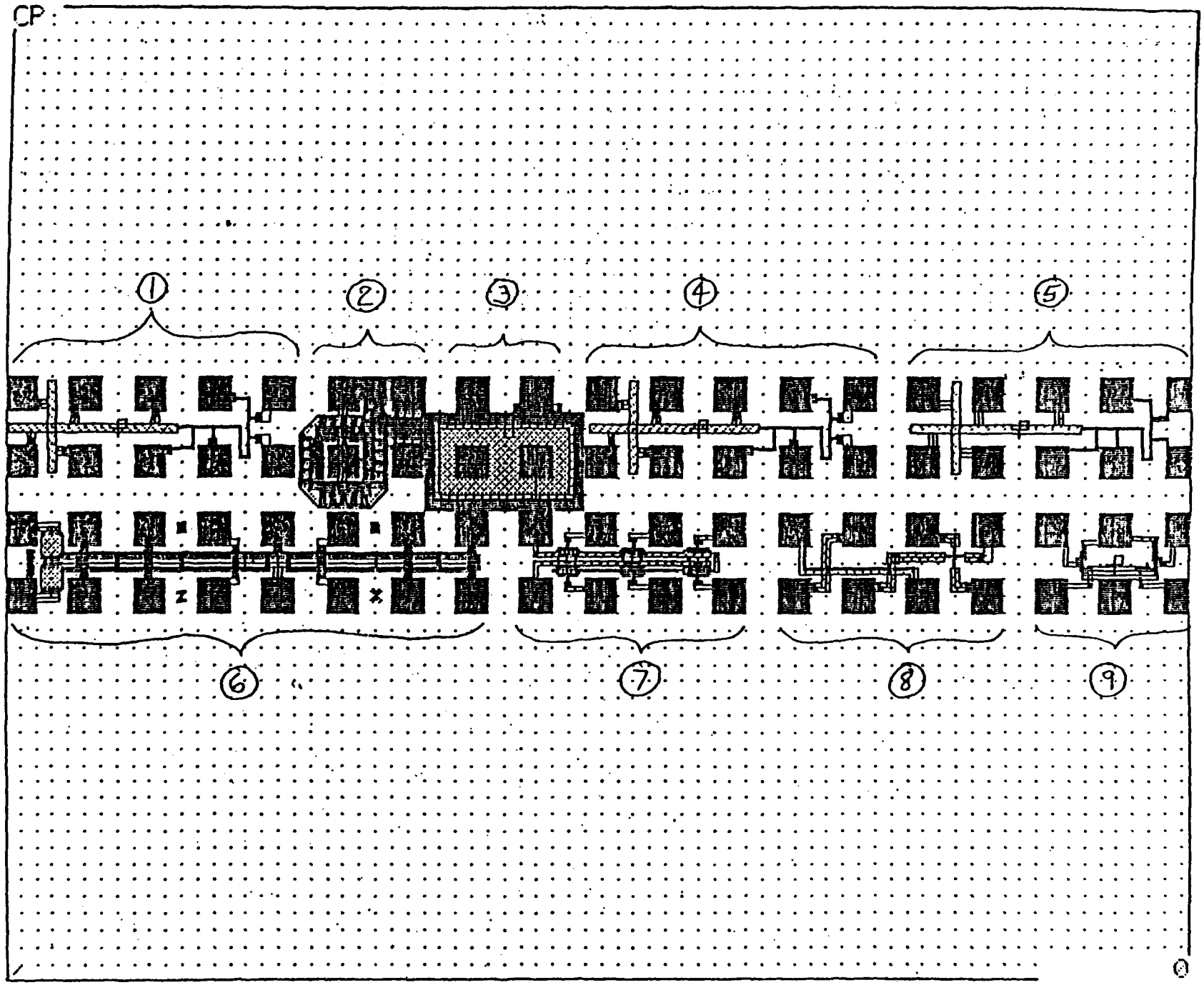
now underway with the objective of testing devices using remote control from the VAX.

In support of the continued development of test masks and testing systems, a study of possible diagnostic prober systems was undertaken. This capability will provide a valuable addition to the present X-Y prober system, as it will permit the diagnosis of individual faults on the chips fabricated in the IC Lab. The diagnostic prober provides the means to measure and inject signal voltages on chip features as small as 2 microns. Therefore, when a chip is found to be nonfunctional, the fault can be localized to a certain region, and the circuit operation of the chip can be proven in detail. This permits a much more precise determination of the true nature of problems which occur on complex VLSI chips. Without this capability, we would be essentially shooting in the dark when trying to determine the cause of problems in chips fabricated in the IC Lab.

The conclusion of the study was that the best choice for our purposes is the MicroManipulator Model 6000 probing system. Example units were evaluated at the local showroom, with an eye to those features necessary for our application. After some discussion with their representatives, they made a very appealing offer of the necessary hardware to us, and the decision was made to purchase an MM 6000 system with accessories for delivery in February of 1982.

In the future, the information provided by Don Ward will be used to design a SPICE parameter extraction chip, and a new test mask will be assembled. This mask will incorporate the basic test structures used in the last NMOS runs, together with the new process verification test strip, the MATRIX yield test chip, and the SPICE parameter chip. Programming of the S3260 and the VAX will continue towards the goal of using ICTEST under remote control for device tests, with preliminary results expected in the Spring. After preliminary

demonstrations of the utility of this connection, the massive task of modifying the S3260 software to run under UNIX will be begun.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FTAF DEVICE RESEARCH

DEPLETED BASE BIPOLAR TRANSISTORS

(Static Induction Transistors)

J. M. C. Stork

During the six month period covered by this report, a Ph.D. Thesis on the viability of the depleted base BJT for VLSI was completed. It analyzes in detail the operation of these devices and provides a clear perspective on their differences and similarities to conventional BJT devices. This report will be published in April 1982. The abstract from the report is reproduced below, by way of summary of the report's contents.

ABSTRACT

An essential characteristic of devices that are viable candidates for VLSI circuits is tolerance of their electrical characteristics to process variations. Because bipolar junction transistors exhibit ideal exponential characteristics, independent of device geometry, they are strong contenders for very fast logic circuits. Scaling introduces heavy doping effects and increases process sensitivity, but conventional devices are relatively tolerant to variations in lateral geometries. Reducing lateral dimensions, however, has led to two-dimensional structures, while the limit on vertical scaling is reached when the basewidth is reduced to zero. Such devices, variably known as depleted-base transistors or bipolar static-induction transitors, have been proposed as alternative structures for high-speed VLSI and, therefore, are the subject of this investigation.

The principles of operation can be described by a widely applicable analytical expression, showing that transport current is controlled by a saddle

point in the potential distribution. Electrical characteristics are specified by the height of the barrier, which is very sensitive to variations in device structure that affect the spacing of the extrinsic base regions. The analytical formulation is complemented by numerical simulations to establish the relationship between barrier height and such processing-related variables as linewidth, junction depth, and doping level. Extreme sensitivity of barrier height to process perturbations is observed, and base efficiency is seen to degrade with lower barriers.

Experimental investigations have verified the theoretically predicted sensitivity of saturation current to linewidth variations by carefully monitoring very small lithographic perturbations. It is also observed that the reduced barrier height in depleted-base transistors leads to less efficient operation and that an electrical p-type base (npn device) is necessary to achieve transconductance comparable to conventional BJTs. Because no direct electrical access to the saddle point of the potential is available, a measurement technique is developed through which the barrier height can be obtained by measuring I/V characteristics as a function of temperature. A theoretical model agrees well with experimental data and identifies the lowering effect of positive depletion charge on the barrier height. The method is especially suited for characterization of novel device structures.

As a result of this work, it is concluded that, although bipolar transistors may play an important role in VLSI circuits, devices such as the depleted-base transistor, whose operation is fundamentally the same but far more process sensitive, are unlikely candidates for such applications.

VLSI MOS DEVICE RESEARCH

(Thao Nguyen)

Research activities on small geometry MOS devices during the period from July 1, 1981 to December 31, 1981 has been performed in the following areas:

- Developing better physical understanding of small geometry effects in MOS devices using 2D Computer Modeling (GEMINI Program) and a 2D analytic Poisson's solution.
- Comparing small geometry effects of standard surface channel (SC-) and buried channel (BC-) MOSFETs based mainly on 2D Computer Simulations.
- Developing detailed physical models for the I-V characteristic and threshold voltage shift in the linear and subthreshold regimes for short channel MOS devices using a 2-D analytic Poisson's solution.
- Characterizing small geometry surface and buried channel devices fabricated in the Stanford I.C. Lab, with dimensions as small as 1.25 μ.

1. Physical Mechanisms responsible for short channel effects in MOS devices:

INTRODUCTION

Short-channel effects in small geometry MOSFETs are well-known and have received considerable attention in the past decade. Several models ranging from simple analytical approximations based on charge sharing concepts [1-3] to empirical relationships [4,5] and sophisticated full three-dimensional numerical analyses [6] have been put forward to predict the dependence of threshold voltage on device physical parameters and have achieved varying degrees of success.

The most familiar models are those based on charge sharing concepts, probably because the concepts are simple. In essence, the charge sharing

models account for the reduction in threshold voltage of short-channel MOS devices through the sharing of the channel depletion region charge between the gate electrode and the source and drain junctions. It is implicitly assumed in these models that the effects of the junctions only extend laterally into the channel a distance equal to the one-dimensional depletion width of the junctions. The channel depletion charge within this depletion width from each junction is then geometrically divided into two parts, one associated with the gate and the other with the junction. Overall charge conservation which equates the total charge on the gate electrode to the total channel depletion charge associated with the gate is then applied to obtain the threshold voltage. The accuracy of these models obviously is critically dependent on how the channel depletion charge is geometrically divided and almost all these models base the charge division upon simple geometry and approximate surface potential arguments.

It has been proposed [7] that a more physically correct explanation of short-channel effects is due to the penetration of the junction electric fields into the channel region. This induces potential barrier lowering, leading to a threshold voltage shift. However, very little specific information about the nature of these junction fields and their role in the threshold shift has been published.

PHYSICAL MECHANISMS RESPONSIBLE FOR SHORT-CHANNEL EFFECTS

Useful physical insight may be achieved from careful examination and interpretation of the fundamental Poisson's equation that governs MOS device operation in the subthreshold regime. Fig. 1 shows the cross section of a short-channel NMOS device with the electric field E and its two components E_x

and E_y at a point in the channel depletion region. The two dimensional Poisson's equation can be expressed as

$$\varepsilon_{si} \frac{\partial E_y}{\partial y}(x,y) + \varepsilon_{si} \frac{\partial E_x}{\partial x}(x,y) = \rho(x,y) \qquad (1)$$

The first term may be interpreted as the gate charge density, qN_G because it has the dimension of a charge density and the vertical component of the electric field E_y mainly originates from the gate electrode. Similarly the second term can be regarded as the junction charge density, qN_J because the lateral component of the electric field E_x mainly originates from the junctions. Thus the net depletion charge density $\rho(x,y)$ can be considered to be the sum of two components qN_G and qN_J. In long-channel devices the electric field in most of the channel region is vertical. Thus E_x and hence qN_J are negligible. By definition of the gate charge density, we have

$$\varepsilon_{si} \frac{\partial E_y}{\partial y} \triangleq qN_G = \rho - qN_J \simeq \rho \qquad (2)$$

the 2-D Poisson's equation thus reduces to the familiar 1-D form. Integrating eq.(2) twice with respect to y from y=0 (surface) to $y = \infty$ to obtain the vertical charge conservation leads to the long channel threshold voltage which is independent of device geometry and bias conditions.

In short-channel devices the lateral junction electric field E_x is non-zero and thus qN_J cannot be neglected in eq. (2). The charge density term is thus less than the net depletion charge ρ. If the junction charge density qN_J were known, equation (2) could be integrated twice with respect to y, keeping x constant, to obtain the vertical component of electric field E_y and the surface potential. The threshold voltage could then be calculated by applying vertical charge conservation at the location of the minimum surface

potential (virtual cathode). Since the junction charge density qN_J is likely dependent on device geometry and bias conditions, so is the threshold voltage.

In comparing short and long channel devices, it can thus be concluded that short-channel devices can be modeled similarly to long-channel devices, but with effectively a more lightly doped substrate. It is the lateral junction field E_x in short-channel devices that causes the smaller gate charge density. As a result of the lighter effective doping, the short-channel threshold is lower than the long channel value. Furthermore it is also to be expected that the vertical depletion width at the virtual cathode point will be larger for short-channel devices because of the lighter effective substrate doping. This will be verified later with computer simulations.

TWO DIMENSIONAL ANALYTIC SOLUTION

The 2-D Poisson equation, which governs short-channel MOS operation in the subthreshold region,has generally been solved numerically [8]. Analytic solutions have proven difficult to obtain, probably due to the complicated structure of typical MOS device cross sections as shown in Fig. 1. By simplifying the geometry to the rectangular area in Fig. 1, and determining appropriate boundary conditions, a general method of solving the 2-D Poisson equation for the potential in the channel region has been developed. This method is capable of treating a typical MOSFET device with gaussian cylindrical shallow junctions and a gaussian channel implant and has been used to obtain analytic solutions for typical MOS structures. It has been found that the lateral junctionfield E_x in the channel region of these devices can be approximated by a function of the following general form

$$E_x \approx E_S \cosh \frac{\pi(L-x)}{W_c + 3t_{ox}} - E_D \cosh \frac{\pi x}{W_c + 3t_{ox}}$$

$$\cdot \quad \text{Sin} \frac{\pi(y + 3t_{ox})}{W_c + 3t_{ox}} \qquad (3)$$

where $\underline{E}_S = [\underline{V}_S, L, \underline{Y}_j, (\underline{W}_c + 3t_{ox})]$, the magnitude of the source junction field Y_j, $(W_c + 3t_{ox})]$, the magnitude of the drain junction field. Both E_S and E_D vary linearly with junction potentials V_S and V_D.

The junction field E_x obviously consists of two components, one associated with the source and the other with the drain which are opposite in direction. In the source-drain direction E_x decreases exponentially from each junction edge with a decay length equal to $(W_c + 3t_{ox})/\pi$ and in the vertical direction E_x exhibits a sinusoidal characteristic with a half wavelength of $(W_c + 3t_{ox})$.

COMPUTER SIMULATION RESULTS AND DISCUSSION

The concept of modeling short channel devices as long channel devices with a more lightly doped substrate is justified in this section. A 2-D device modeling program GEMINI [8] which solves the nonlinear Poisson equation including electron and hole concentrations was used. The initial device simulated was similar to Fig. 1 with L = 1 μm, $N_A = 1 \times 10^{16}/cm^3$, t_{ox} = 400 A , X_j = 0.2μm, and Y_j = 0.3 μm. The uniform substrate doping was used initially to facilitate comparison with 1-D theory and should not affect the generality of the conclusions. Later simulations will involve implanted channel devices.

Fig. 2 shows the normalized net depletion charge density as a function of distance from the surface in the virtual cathode plane. The drain voltage V_D is varied from 0 to 10 V with steps of 2.5 V. Also shown is the box charge distribution obtained from simple 1-D depletion approximation theory. It is obvious from this figure that the depletion width increases with higher drain voltage and is only reasonably approximated by 1-D theory at V_D = 0 V. This

increase is neither due to an increasing surface potential introduced by short-channel effects (because V_G was decreased for larger V_D to maintain a constant surface potential at the virtual cathode point) nor due to punch-through effects.

The increase in depletion width, however, can be readily anticipated by inspecting Fig. 3 which plots the normalized gate charge density or the normalized effective substrate doping versus distance for the same conditions. At larger V_D the gate charge density becomes smaller. This is due to higher lateral junction fields and hence larger junction charge density. Because of the lower effective substrate doping the depletion width is larger. Thus these results have verified that short-channel effects can be modeled as a reduction in the effective substrate doping. They also point out the inaccuracy of charge sharing models which assume the middle region of the channel is governed by 1-D theory. The threshold voltage shift with larger V_D is also apparent in Fig. 3. Since the surface potential at the virtual cathode is the same for all drain voltages, the threshold shift is proportional to the reduction in the depletion charge per unit area which is directly related to the area under the curves of Fig. 3. This area is clearly smaller for larger V_D despite the larger depletion width.

The functional behavior and properties of the lateral junction electric field E_x are now described with the results obtained from computer simulation of an implanted channel MOSFET, whose cross-section is shown in Fig. 4. This device has a threshold shift implant with $Q = 3 \times 10^{11} cm^{-2}$ $R_p = 750$ A and $\sigma = 1000$ A, and $L = 2$ μm, $X_j = 0.2$ μm, $Y_j = 0.3$ μm, $t_{ox} = 400$ A and $N_A = 5 \times 10^{15}$ cm^{-3}.

Fig. 4 also shows the lateral junction field E_x as a function of distance from source to drain along the line HH'. The source and drain fields are

symmetrical about the virtual cathode plane because of the zero drain voltage. It is clear that the junction fields decay exponentially with distance from the junction edges. 1-D theory would predict the junction fields decrease linearly within the depletion region and exponentially beyond the depletion edge with a decay length equal to the extrinsic Debye Length. The decay length of E_x is not related to the substrate Debye length but rather to the effective depth of the channel depletion region. Its value from computer simulation agrees with $(W_c + 3t_{ox})/\pi$ as predicted from the analytic solution. Because of their exponential nature, the junction fields will penetrate throughout the channel depletion region regardless of the channel length, but will be important only in short channel devices. This also indicates a limitation of charge sharing models which assume the junction effects extend only up to a distance equal to the 1-D junction depletion width.

Fig 5 shows the lateral junction field E_x versus distance from source to drain for three different bias conditions. The gate voltage has been adjusted so that the minimum surface potential is the same for all cases. The junction field with back gate bias, curve (B), shows a similar behavior as for zero back gate bias, curve (A), except for a larger decay length. This is to be expected because back gate bias increases the channel depletion width W_c. As a result of the larger decay length the magnitude of E_x is two orders of magnitude larger near the virtual cathode point which therefore results in a lower effective substrate doping and larger short channel effects. For non zero drain voltage, curve (C), the source junction field is unchanged but the magnitude of the drain junction field is increased by more than one order of magnitude. The decay length is,however, unaffected by the drain voltage because a much larger V_D is needed to significantly increase the depletion width W_c for $L = 2$ μm. The virtual cathode point where the source and drain junction fields exactly

cancel each other is shifted towards the source junction because of the larger drain junction field. Simulation of shorter L devices showed, as expected, that the magnitude of E_x near the virtual cathode point is much larger. The decay length does not increase dramatically because W_c does not change substantially. The simulations also revealed that E_x displays the positive half sinusoidal shape in the vertical direction predicted by the analytic solution.

It follows from the definition of junction charge density that N_J should have the same functional behavior as E_x. The minimum value of N_J at the virtual cathode point which determines the threshold voltage shift is exponentially dependent on the ratio of the junction-virtual cathode point distance to the decay length. This ratio is directly related to the aspect ratio of the channel region $L/(W_c + 3t_{ox})$. Thus the threshold voltage shift is critically dependent on the channel aspect ratio. The smaller it is the larger the short-channel effects become.

2. A Comparison on short-channel effects of SC and BC MOSFETs

The Buried Channel MOSFET (BGMOSFET) is a relatively new MOS device structure proposed by Nishiuchi, et. al. [9] as an alternative to VLSI devices. BCMOSFET, as shown in Fig. 6, is similar to a depletion load MOSFET except that the polysilicon gate is doped with p-type and n-channel implant dose is much lower so that the positive flatband voltage obtained from the p-type gate can pinch the channel off at equilibrium and thus make the BCMOSFET an enhancement mode device.

Because the current channel in this structure occurs below the surface (and hence the name bvuried channel), the device exhibits several attractive properties such as:

- High carrier mobility
- High drain breakdown voltage
- Smaller hot electron effects

These properties have generally been accepted and confirmed with both experimental data and computer simulations [9,10]. It may therefore be concluded that BCMOSFETs are high performance devices. However, the notion that BCMOSFETs are a viable candidate for VLSI devices is still questionable [11] because an even more important requirement than high performance for VLSI applications is a small sensitivity of device electrical characteristics to processing variations, i.e., a small dependence of threshold voltage and current on device geometry and bias conditions. The potential of BCMOSFETs in VLSI circuits can thus be investigated by comparing the short channel effects of conventional (SCMOSFET) and buried channel (BCMOSFET) devices.

COMPUTER SIMULATION RESULTS

A theoretical comparison has been performed through extensive use of the GEMINI program. Both SC and BC MOSFET devices with identical geometry and equivalent doping profiles have been simulated and their threshold voltage shift in the linear regime and their subthreshold characteristics have been examined. The results shown in subsequent figures are for devices with the following parameters: t_{ox} = 400 A, X_j = 0.2 μm, Y_j = 0.3 μm and $N_A = 5 \times 10^{15}$ cm^{-3}. The channel implant has R_p = 750 A, $N_p = 2 \times 10^{16}$ cm^{-3} and junction depth of 0.2 μm.

Figure 7 shows the calculated linear threshold voltage shift as a functon of channel length L. It is clear that the BCMOS performance is better than that of SCMOSFET in the linear regime (strong inversion for SCMOS, strong accumulation for BCMOS). This can be attributed to the fact that the BCMOS source/drain junction depth is effectively reduced by the n-channel region. Thus the two dimensional effects in the channel depletion region are smaller than in the SCMOD device.

Figs. 8 and 9 compare the calculated substhreshold shift in V_G at $I = 10^{-2}$ A for W/L = 1 (i.e. the lateral shift in the subthreshold I-V characteris-

tic) as the channel length L decreases at small V_{DS} and as V_{DS} increases at L = 1 μm, respectively. In this regime, the BCMOS device shows greater sensitivity to device dimensions and drain bias, which can be predicted because the BCMOS depletion region under the gate is deeper as a result of the n-channel region and the larger potential barrier of the channel-substrate junction. This implies a poorer aspect ratio of the channel region and thus larger short-channel effects. Fig. 10 shows the subthreshold inverse slope at threshold condition as a function of decreasing channel length L. While the long channel slope of the two devices is about the same, the short channel (L < 2 μm) slope of BCMOSFET is worse. The capacitance coupling between the source/drain junctions and the virtual cathode, which is responsible for the increase in slope of both devices at small L, is larger for BCMOS devices because of its deeper depletion region.

It has also been discovered that the subthreshold characteristic of BCMOSFETs exhibits a constant leakage current as shown in Fig. 11, which is no generally present in SCMOS devices. The origin of this leakage current has been thoroughly investigated both experimentally and theoretically. It has been found that surface inversion leads to this leakage current. As the gate voltage is decreased, the surface potential decreases and eventually becomes strongly inverted. The large hole concentration at the surface shields the gate from further control over the potential barrier that controls the subthreshold current and this results in a constant leakage current, independent of gate voltage. From the theoretical analysis, the potential maximum at the surface inversion condition is a consequence of a junction-type implanted channel device. It is never equal to zero and its value is determined by implant parameters and substrate concentration.

Hence it can be concluded from the above comparison that while the n-type implanted channel helps to reduce the BCMOS short-channel effects in the linea regime, the same implanted channel adversely degrades the BCMOS subthreshold performance in three aspects: larger sensitivity to drain voltage, poorer subtheshold slope and a constant leakage current.

Historically the turn-on region ($V_{GS} \geq V_T$) has been the region of operation of most importance for MOS devices and circuits but for the last decade the turn-off regime has received more and more attention. Among many reasons for this change has been the development of new MOS circuits in which the performance was critically dependent on the subthreshold leakage current. Some of these new circuit techniques have become increasingly widely used in VLSI systems such as the use of an MOS device as a transfer gate in dynamic circuits (Dynamic RAMs, gate arrays). Thus poor subthreshold performance may impact long-term scalability.

For the reasons mentioned above, the improved BCMOS performance in the linear regime may not be sufficient to justify the BCMOSFETs as a viable contender for VLSI devices unless the inferiority of the BCMOS subtheshold regime can be minimized. The most effective way of improving all three subthreshold parameters is to minimize the n-type implanted channel depth. Computer simulations of the same SC and BC MOSFETs except for the channel R_p being reduced by 50% have shown that the gap between BCMOS and SCMOS subthreshold performance was narrowed as predicted. However, the BCMOS performance in the linear regime was worsened and the BCMOS advantage seemed to disappear. If the channel depth is decreased further, then it is to be expected that the BCMOS device will not be better than the SCMOS device in both regimes: the reduction in the BCMOS source/drain junctions cannot offset the effects of a deeper depletion region due to the higher potential barrier of the channel

substrate junction; this leads to a larger linear threshold voltage shift. The BCMOS subthreshold performance can only approach but never be equal to or better than that of SCMOS devices. Besides, the attractive features associated with buried channel conduction may disappear for very shallow channels and the device may suffer reproducibility problems due to low energy implants.

In summary, based on the comparison fo short channel effects in BCMOS and SCMOS devices it is concluded tha BCMOSFETs are unlikely to find widespread us in VLSI circuits. However, the physical understanding of their performance limitations will be very useful in understanding depletion load devices which are very similar in operation to the BCMOS device.

It should be kept in mind that the two devices (BCMOSFET and SCMOSFET) under comparison have identical geometries, doping profiles and bias conditions. The above comparison only deals with devices in bulk silicon, thus the various results obtained above may not be necessarily valid for devices on insulator substrates where the channel depletion depth is limited. Finally, the above comparison is based mainly on 2-D computer simulations because a rigorous experimental comparison would require the fabrication of surface and buried channel devices with identical geometries, side by side on the same chip. The available experimental devices were fabricated on separate wafers because of differences in the fabrication process for SCMOS and BCMOS structures. Thus physical parameters are now identical (linewidths, doping profiles, etc.), which makes definitive experimental comparison difficult. We will be investigating and characterizing these devices in the near future, however, to at least qualitiatively verify the theoretical results.

3. Physical Models for Short Channel MOSFET I-V Characteristic and Threshold Voltage:

The development of a general 2-D analytic solution of Poisson's equation opens up many opportunities for theoretical analyses of short channel device

characteristics, which do not require solving the current-continuity equation simultaneously with Poisson's equation. Among such device characteristics are linear regime current, subthreshold current, threshold voltage, bulk punch-through current and voltage, drain induced barrier lowering effects. Thus far the analytic Poisson's solution has been used to derive 2-D models for the short channel SCMOS drain current in both the linear and subthreshold regions. The threshold voltage shift in both regions also comes out as a by-product of the derivation. The results are very encouraging and show that 2-D calculations of bulk punch-through characteristic are no longer only a remote possibility and that a 2-D analytic model of short channel drain current in the saturation region is no longer viewed as an impossible task. The above models, if proved to be successful, could greatly impact our understanding of MOS device physics. While these models must still be verified with computer simulation and experimental data, some of the interesting results are summarized below:

- Linear regime I-V Characteristic:

-- The short channel I-V relationship takes the same form as the long channel one, except for a negative threshold voltage shift ΔV_{TLIN}.

-- When the channel length is not too short, ΔV_{TLIN} agrees with the results obtained from charge sharing models (such as Yau's model) which are known to be reasonbly accurate for relatively long L, but poor at shorter L. ΔV_{TLIN} in this case exhibits a (1/L) dependence.

-- The 2-D model not only justifies the main assumption used in charge sharing models (i.e. the overall charge neturality) to explain why such models work for long L but also spells out the limits of these models and when the fail for short L.

- Subthreshold Regime I-V Characteristic

-- The short channel I-V relationship takes the same form as the long channel one except that the following parameters take a different value: the effective depth of the surface inversion layer W_{eff}, the effective length of the device L_{eff}, the subthreshold inverse dope n and the threshold voltage shift ΔV_{TSUB}.

-- W_{eff} is approximately proportional to the reciprocal of vertical surface field, thus W_{eff} increases as L decreases.

-- L_{eff} is inversely proportional to the curvature of the potential at the virtual cathode, thus L_{eff} can be much less than the metallurgical length for very short L.

-- n is larger at small L because of the increasing capacitance coupling between the junctions and virtual cathode.

-- ΔV_{TSUB} is related to drain induced barrier lowering effects and also causes the most significant change in the subthreshold I-V curve, ΔV_{TSUB} is different from ΔV_{TLIN} in that it does not exhibit (1/L) dependence for large L but decreases exponentially at short L. This is a surprising result because it has been shown [12] that for long channel devices, the linear threshold voltage is very close to the threshold voltage obtained from subthreshold current. This is often assumed valid for short channel devices, and as a result, two threshold voltages are used indifferently. The difference in the two threshold voltages of short-channel devices can be attributed to the difference in the conduction mechanism (drift in linear regime and diffusion in subthreshold regime) and the two dimensional effects on the surface mobile charge.

4. Short-Channel Device Characterization:

Several surface channel and buried channel MOS test chips with minimum mask dimension down to 1.25 μm were fabricated before the I.C. Lab was shut

down for renovations and equipment modifications. These test chips were designed to provide experimental data for the device physics and modeling efforts on th short-channel effects.

Device measurements and characterization are still in progress, but results obtained thus far show that both SCMOS and BCMOS devices work for all gate lengths. The smallest devices have an electrical channel length of about 0.25 μm (as compared to the nominal mask length of 1.25 μm) and exhibit severe short channel effects as would be expected. (The constant leakage current observed in BCMOS and depletion load devices as mentioned in section 2, has been fully investigated.) Measurements and characterization of these devices will continue over the next several months to verify the modeling results described above.

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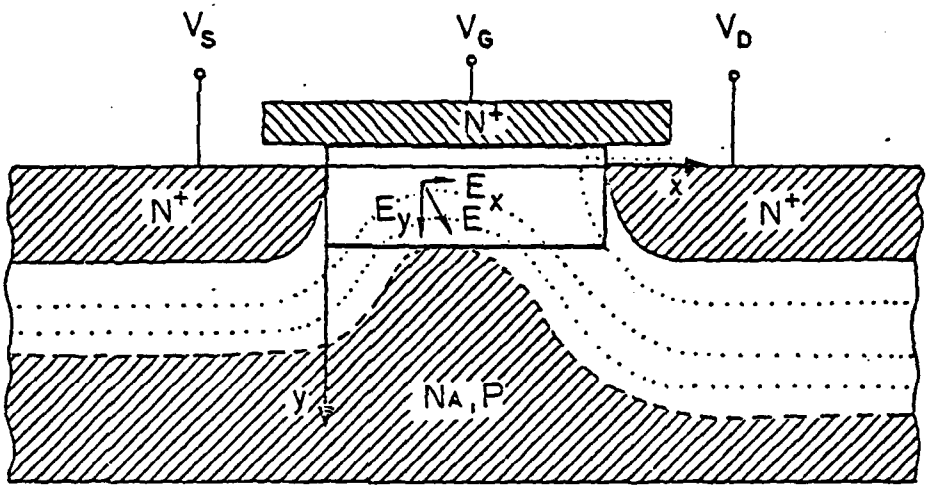


SHORT-CHANNEL MOSFET

Fig. 1: Cross section of typical small geometry NMOS transistor.

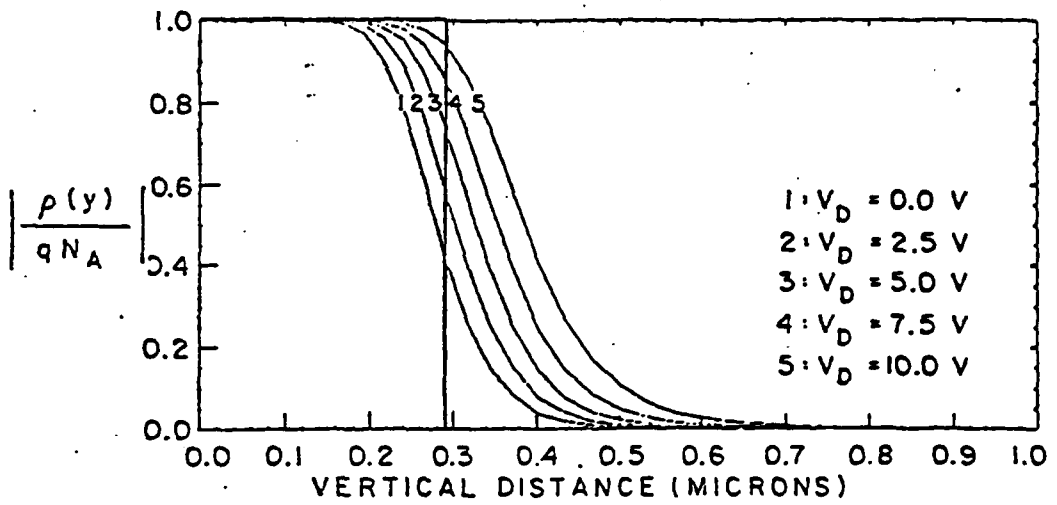


Fig. 2: Calculated normalized depletion region charge density vs depth for a 1 μm channel length device.

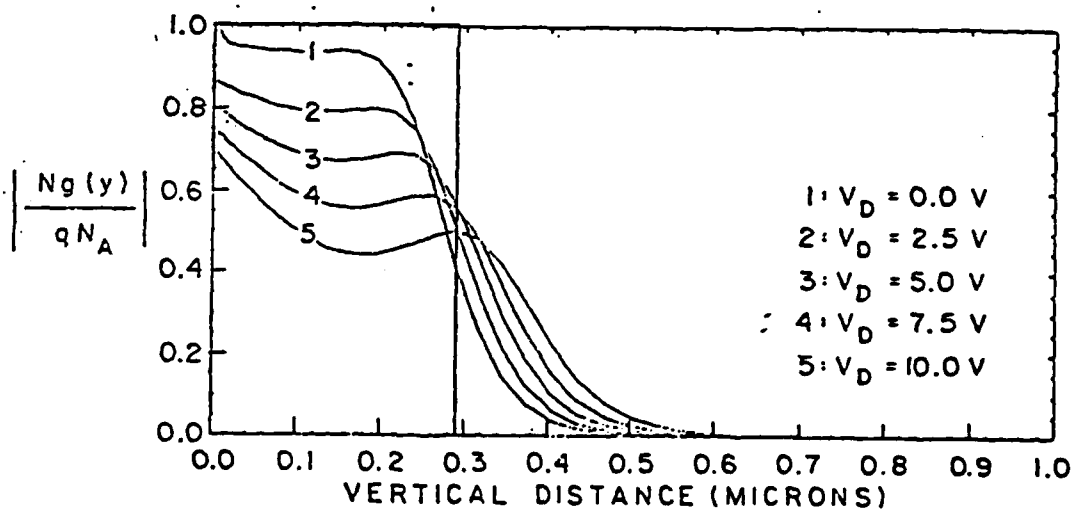


Fig. 3: Calculated normalized gate supported charge density in the depletion region vs depth for the device in Fig. 2.

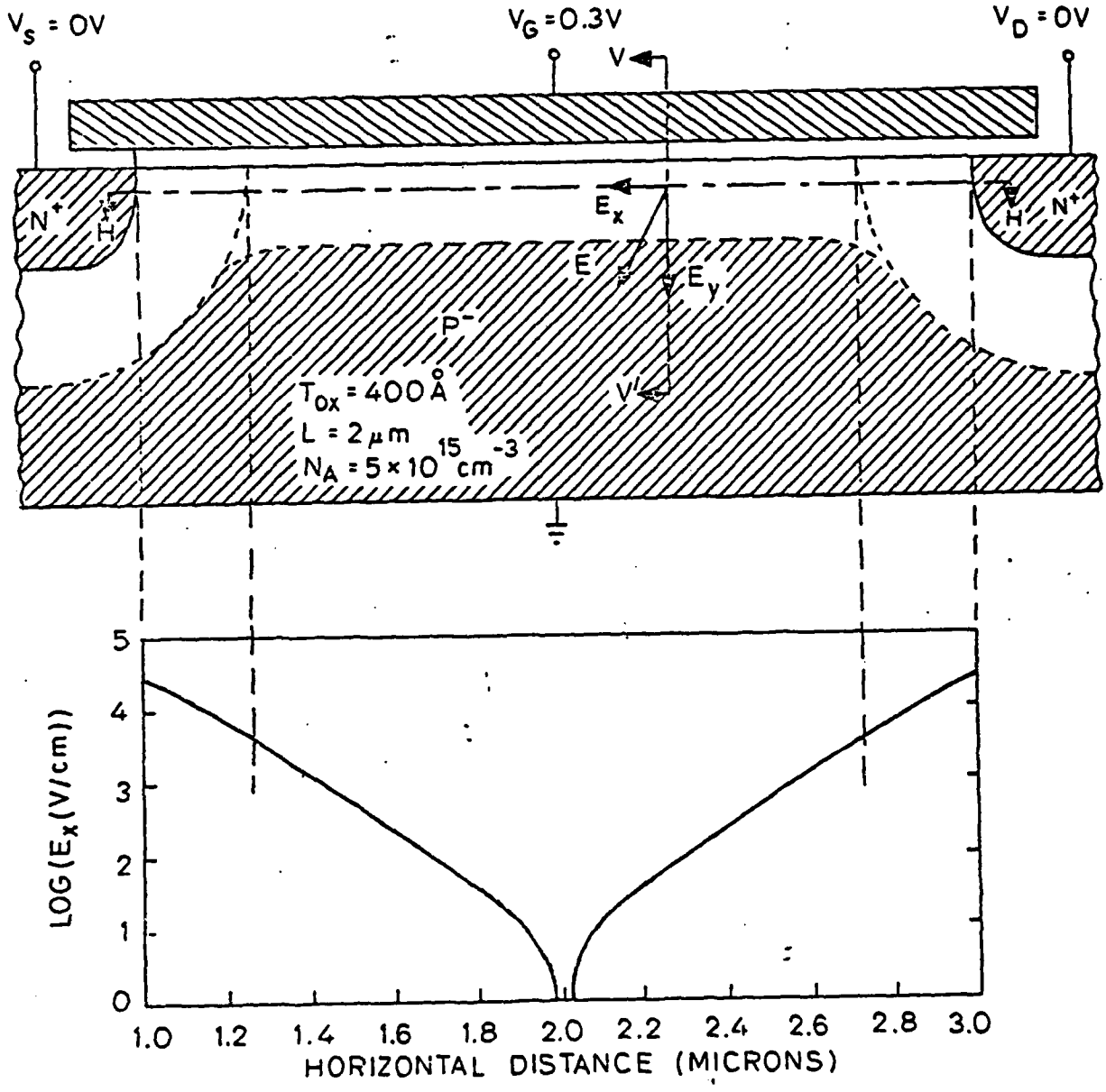


Fig. 4: Implanted channel MOSFET. a) Simulated structure. b) E_x along HH'.

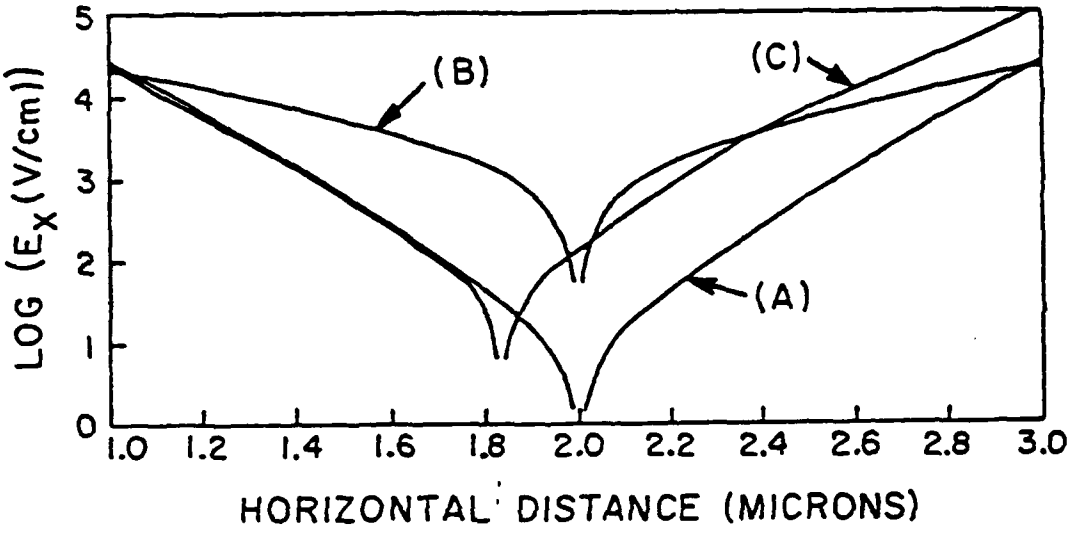


Fig. 5: E_x vs distance for a) $V_D = V_{sub} = 0V$, $V_G = 0.3V$ (as in Fig. 4)
b) $V_D = 0V$, $V_{sub} = 2.5V$, $V_G = 0.925V$
c) $V_D = 2.5V$, $V_{sub} = 0V$, $V_G = 0.3V$

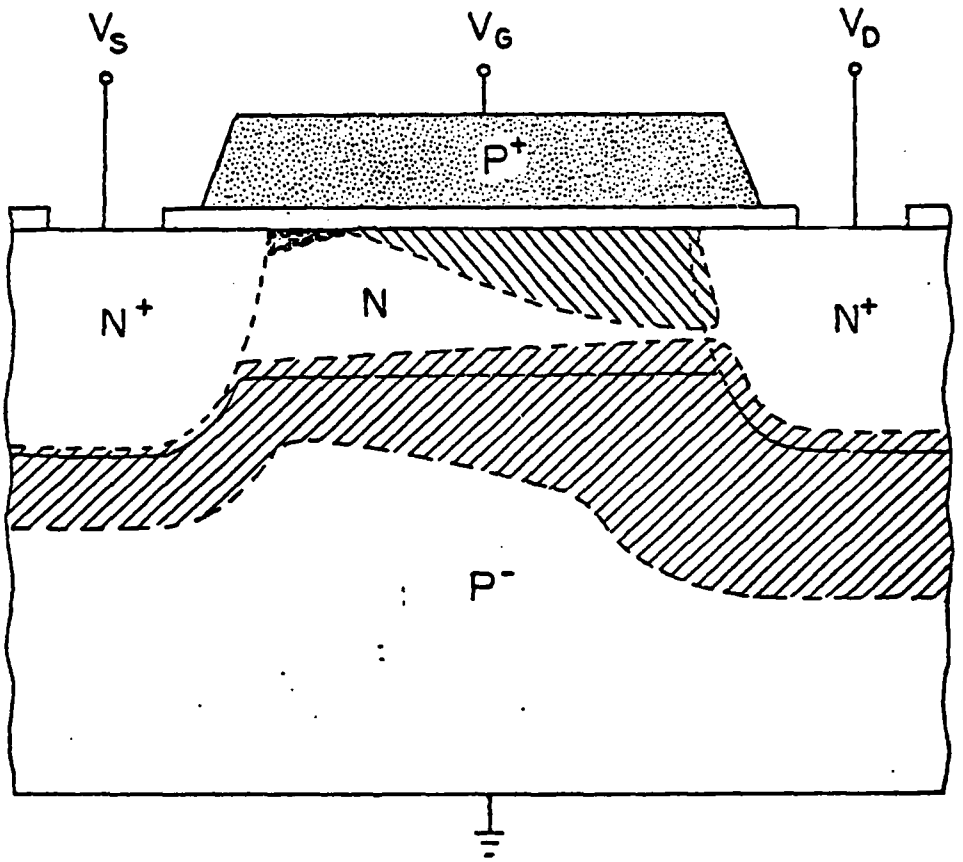


Fig. 6: Cross section of a buried-channel MOS transistor

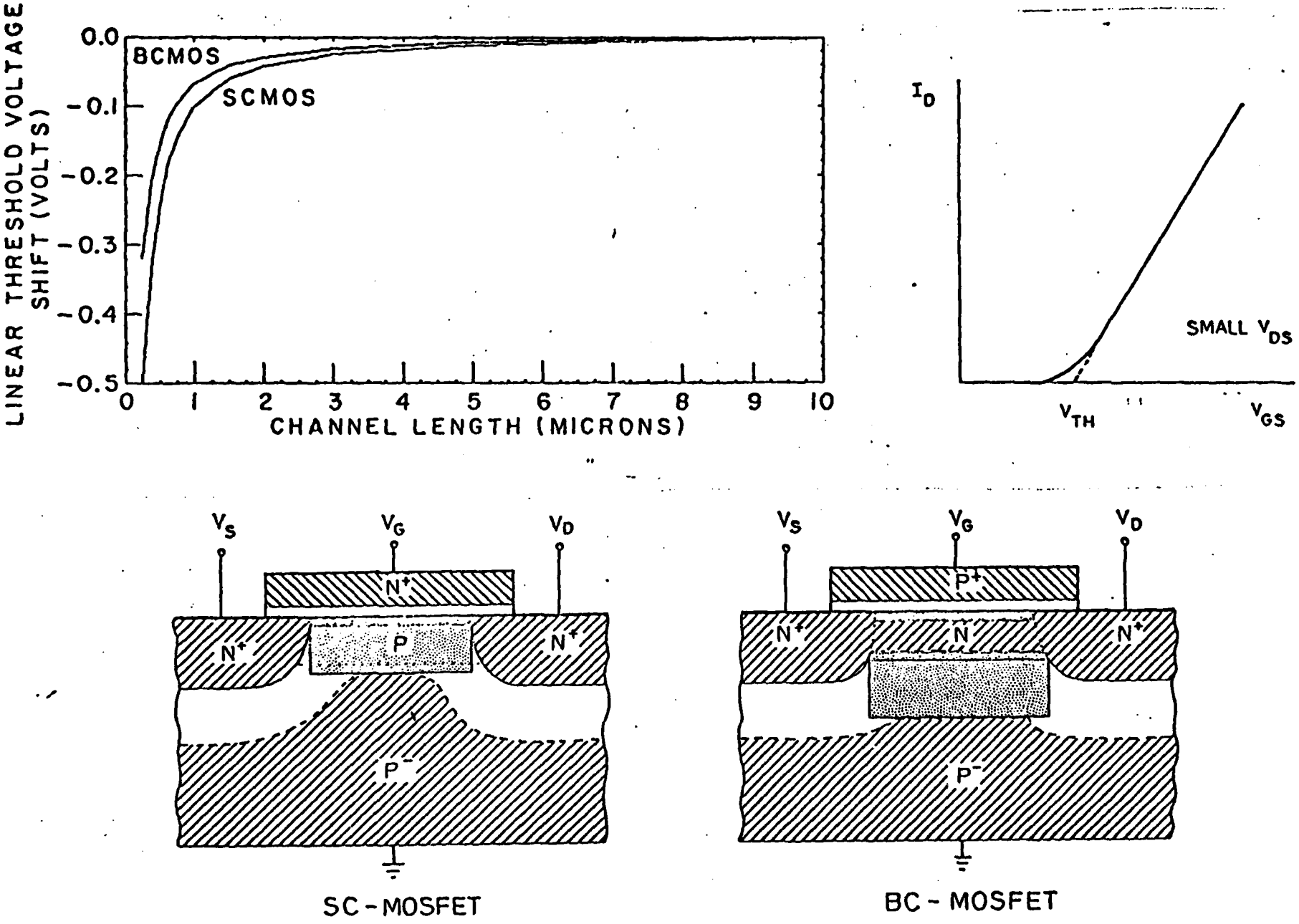
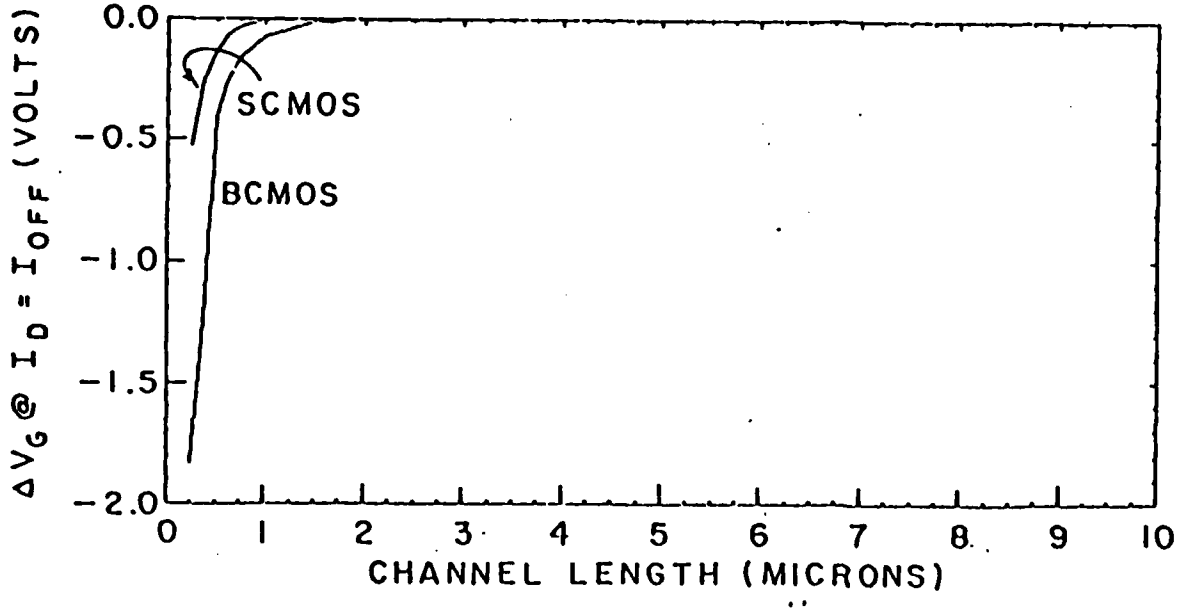
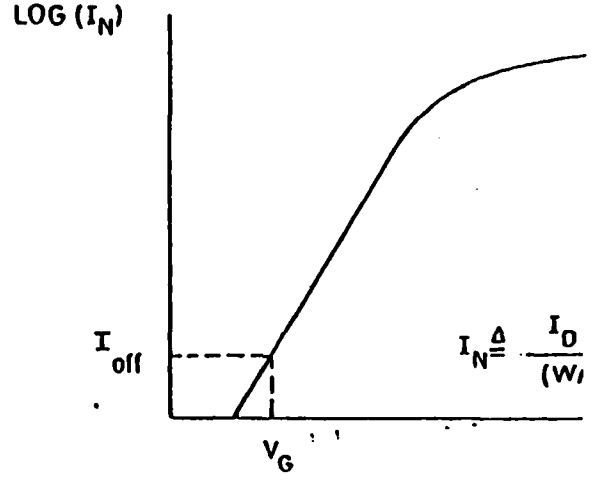


Fig. 7: Linear region threshold voltage shift vs L for BCMOS and SCMOS devices.





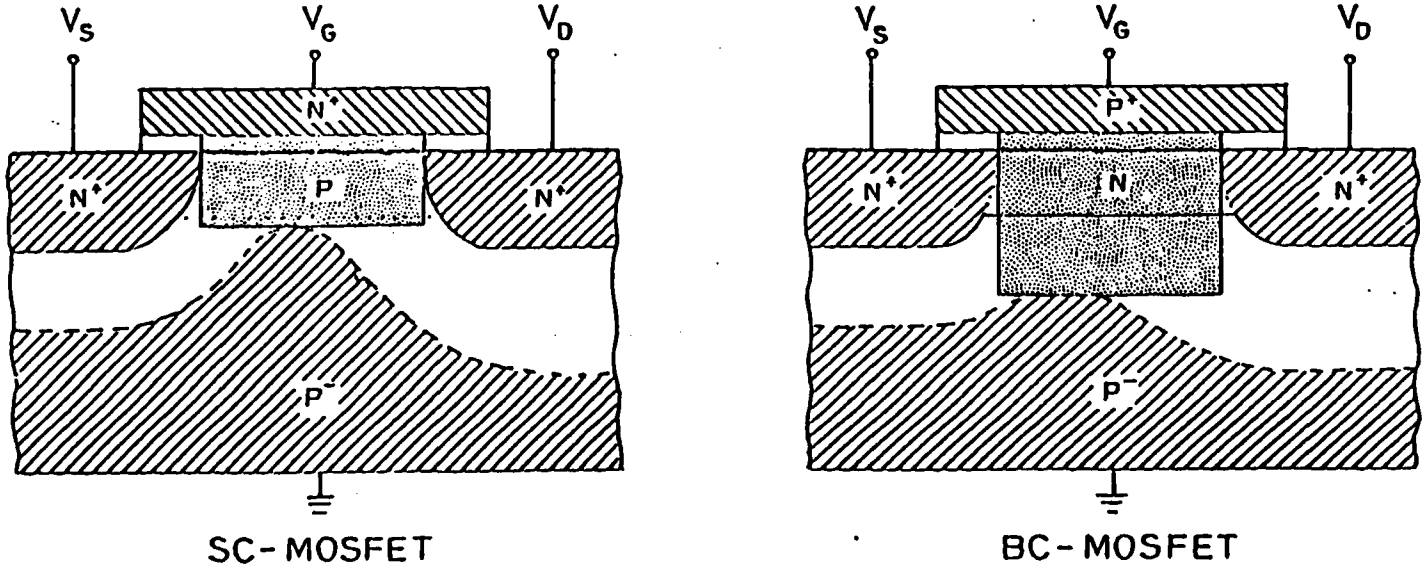
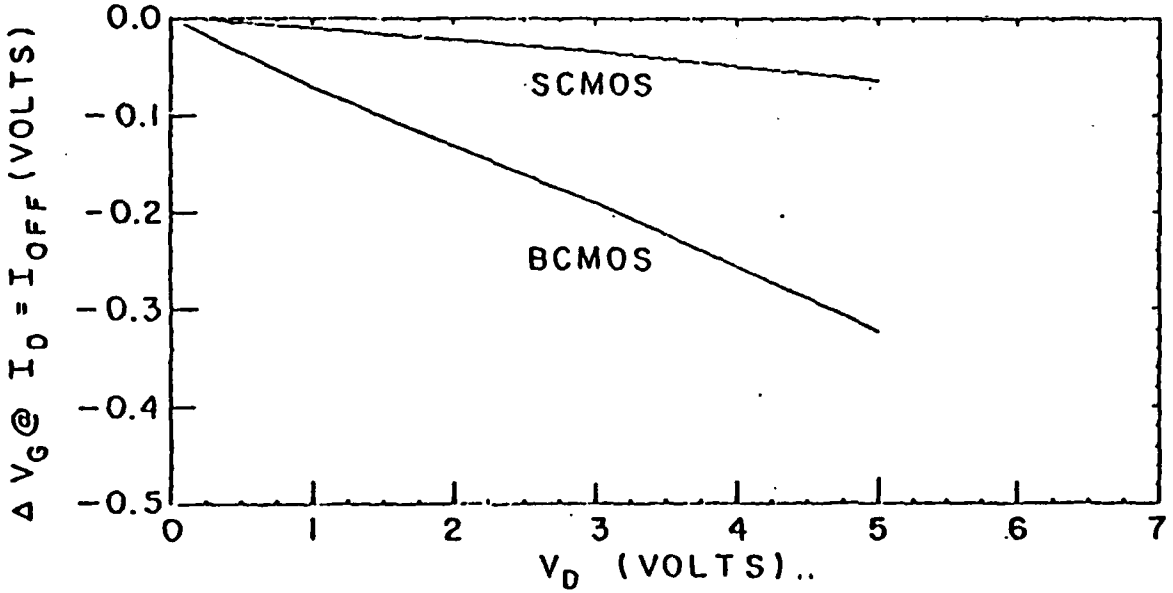
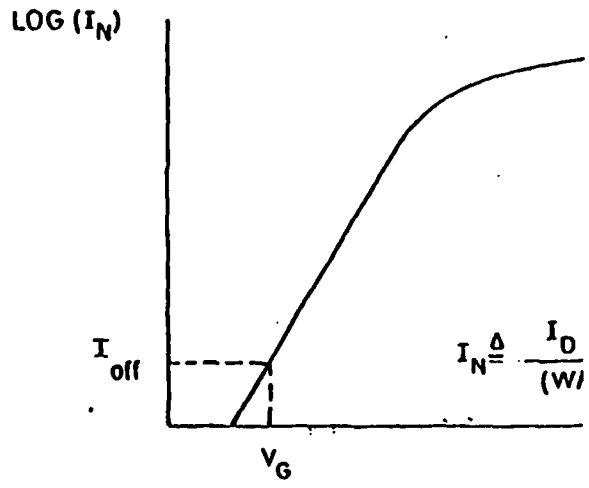


Fig. 8: Lateral shift in gate voltage at $I = I_{off}$ (10^{-12}A) vs L for BCMOS and SCMOS devices.





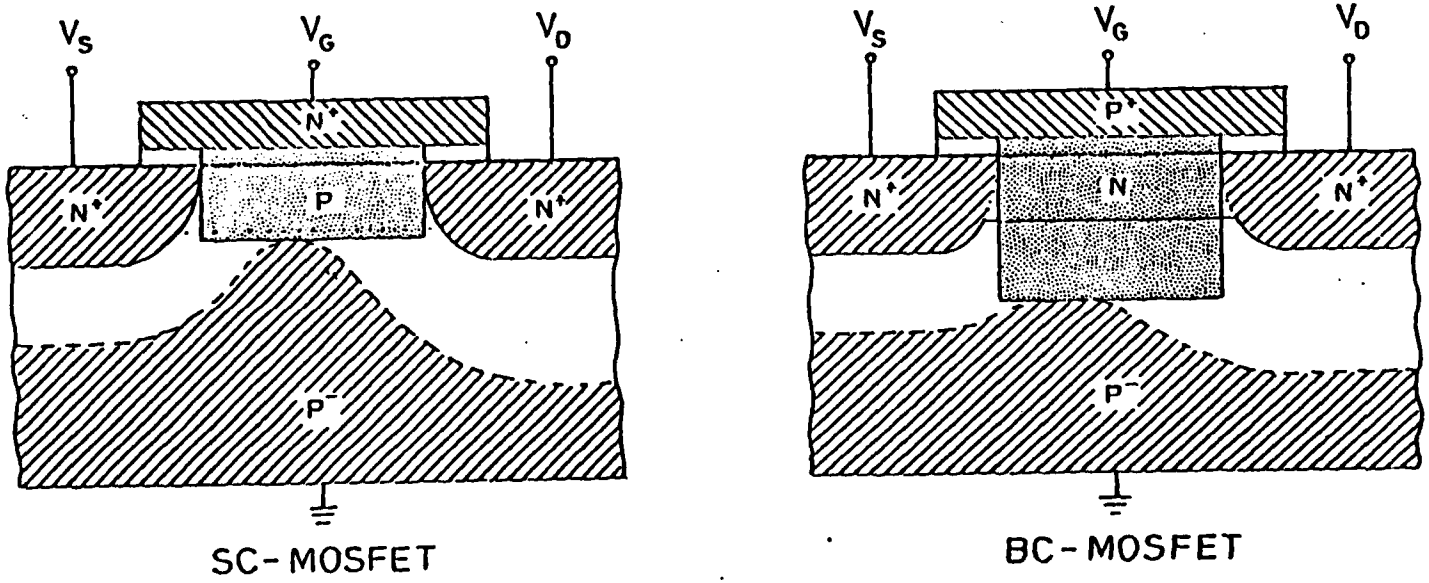


Fig. 9: Lateral shift in gate voltage at $I = I_{off}$ (10^{-12}A) vs V_D for BCMOS and SCMOS devices.

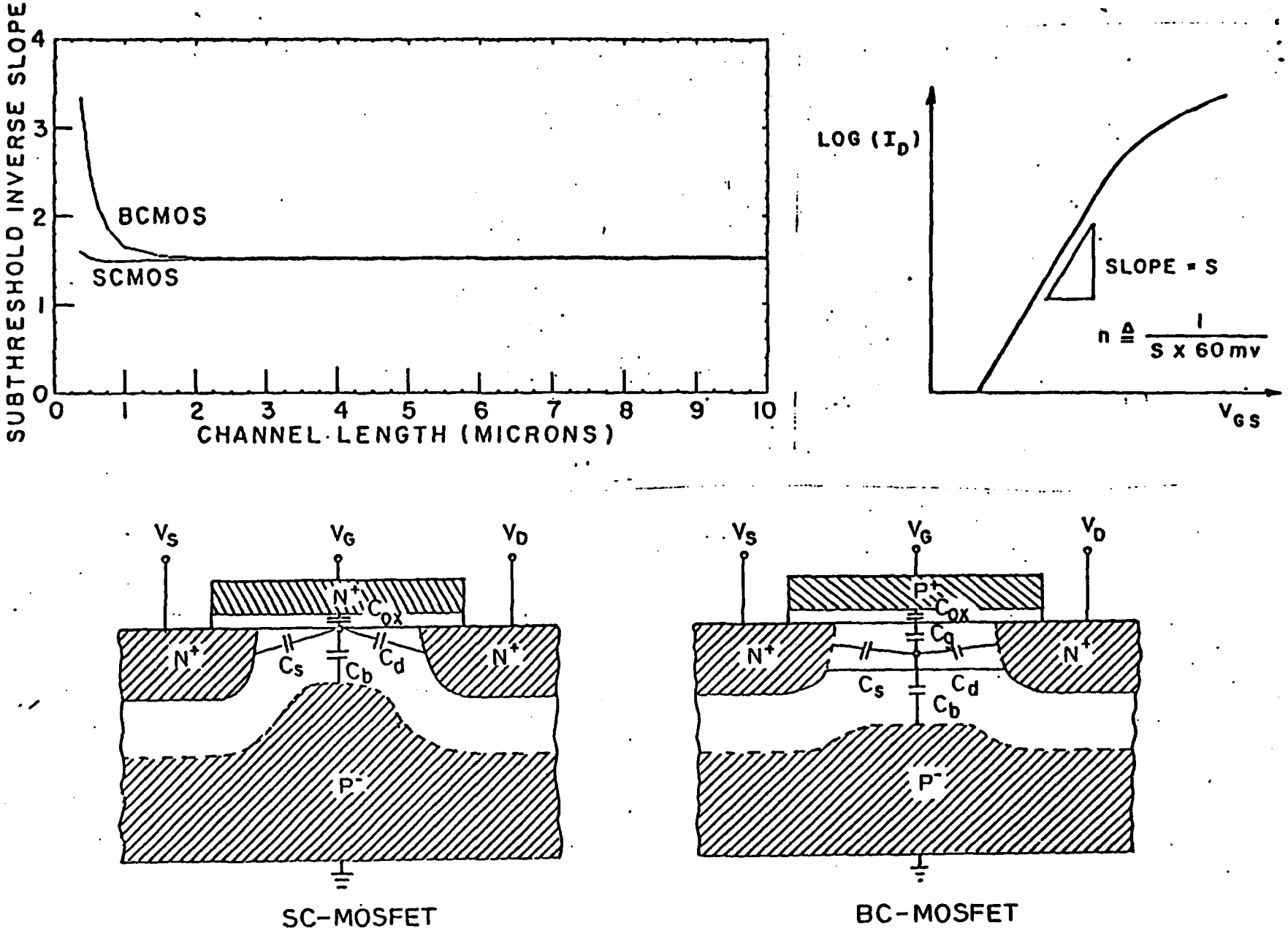


Fig. 10: The subthreshold inverse slope vs L for BCMOS and SCMOS devices.

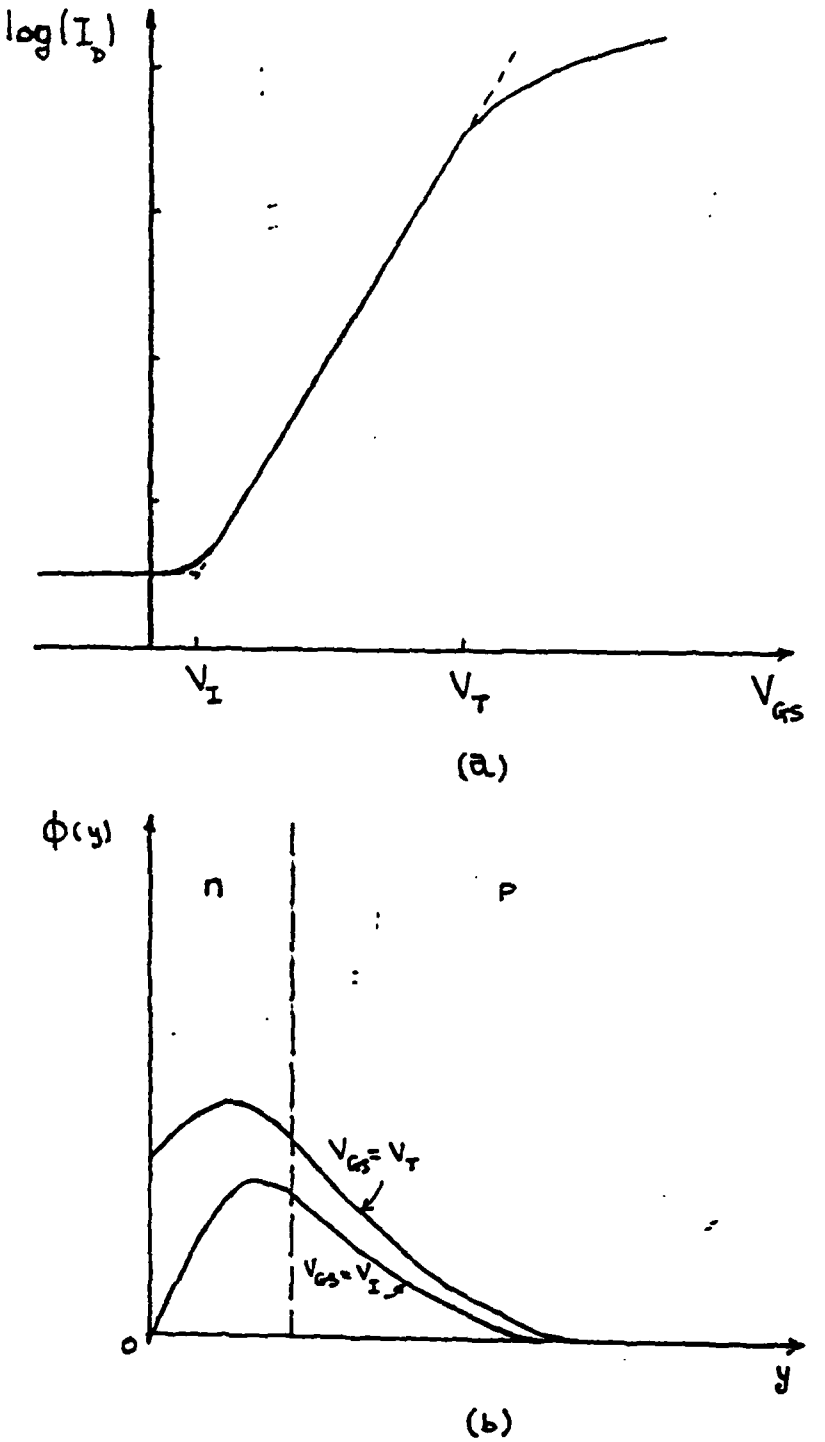


Fig. 11: (a) Subthreshold leakage current in BCMOS devices.
(b) Potential distributions in the virtual cathode plane for $V_{GS} = V_T$ and $V_{GS} = V_I$.